

PAIDC

QUERY CONTROL FORM		RTIS USE ONLY	
Application No. <u>091925,102</u>	Prepared by <u>NH</u>	Tracking Number <u>05888489</u>	
Examiner-GAU <u>Dang - 2818</u>	Date <u>1-29-04</u>	Week Date <u>01/12/04</u>	
	No. of queries)	IFW	

JACKET

a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

- a. Page Missing
- b. Text Continuity
- c. Holes through Data
- d. Other Missing Text
- e. Illegible Text
- f. Duplicate Text
- g. Brief Description
- h. Sequence Listing
- i. Appendix
- j. Amendments
- k. Other

CLAIMS

- a. Claim(s) Missing
- b. Improper Dependency
- c. Duplicate Numbers
- d. Incorrect Numbering
- e. Index Disagrees
- f. Punctuation
- g. Amendments
- h. Bracketing
- i. Missing Text
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- k. Other

MESSAGE

PTO-1449: Please either initial or line through citations. Copy provided for reference.

Thank you

initials N.H.

RESPONSE

initials

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial N	
				M-11822 US		09/925,102	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)		RECEIVED	
(Use several sheets if necessary)				Jack H. Yuan et al.		JUL 30 2002	
				Filing Date		Group Technology Center 2100	
				August 8, 2001		2185	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AP	6,151,248	Nov. 21, 2000	Harari et al.			
	AQ	6,222,762	Apr. 24, 2001	Guterman et al.			
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AR -	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.					
	AS -	Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.					
	AT	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.					
	AU	Hori et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," <i>IEDM 92</i> , April 1992, pp. 469-472.					
Examiner			Date Considered				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,043,940	Aug. 27, 1991	Harari			RECEIVED JUL 30 2002 Technology Center 2100	
	AB	5,070,032	Dec. 3, 1991	Yuan et al.				
	AC	5,095,344	Mar. 10, 1992	Harari				
	AD	5,172,338	Dec. 15, 1992	Mehrotra et al.				
	AE	5,297,148	Mar. 22, 1994	Harari et al.				
	AF	5,313,421	May 17, 1994	Guterman et al.				
	AG	5,315,541	May 24, 1994	Harari et al.				
	AH	5,343,063	Aug. 30, 1994	Yuan et al.				
	AI	5,661,053	Aug. 26, 1997	Yuan				
	AJ	5,712,180	Jan. 27, 1998	Guterman et al.				
	AK	6,103,573	Aug. 15, 2000	Harari et al.				
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AL	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.						
	AM	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.						
	AN	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.						
	AO	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.						
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Application No. <u>09/950,959</u>	Prepared by <u>N.H.</u>	Tracking Number <u>05884677</u>	
Examiner-GAU <u>Le-2858</u>	Date <u>1-29-04</u>	Week Date <u>01/05/04</u>	
	No. of queries <u>1</u>	<u>JFW</u>	

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	initials <u>N.H.</u>
	RESPONSE
	initials

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Atty. Docket No.

C000400

Serial No.

09/950,959

Applicant

Robert L. Dickerman et al.

Filing Date

September 12, 2003

Group

2858

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	4,914,378	4/90	Hayashi et al.			
	4,656,595	4/87	Hognestad			

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation	
WO 01/94876	12/01	WIPO			Yes	No
0 277 467	10/88	EP				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Page, Etc.)

		PCT International Search Report dated 24/10/2003
		Horowitz P and Hill W.: "The Art of Electronics" Cambridge University Press, Cambridge, XP002246138, ISBN: 0-521-37095-7 - See argumentation against the unity of the application - Page 223 - Page 224

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DATE CONSIDERED

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